WHAT IS CLAIMED IS:

1. Variable gain amplifier for amplifying a radio frequency signal by using a field effect transistor for signal amplification, said variable gain amplifier comprising:

an input impedance correcting means for correcting the input impedance when varying the gain at the input side of the field effect transistor for signal amplification;

an output impedance correcting means for correcting the output impedance when varying the gain at the output side of the field effect transistor for signal amplification; and

an amplifier bypass means for passing the radio frequency input signal to the output side by skipping the field effect transistor for signal amplification when varying the gain.

2. Variable gain amplifier for amplifying the radio frequency signal by using a field effect transistor for signal amplification, in which the field effect transistor for signal amplification is of dual gate type, and a first gate terminal is connected to a radio frequency signal input terminal by way of a DC cut capacitor at input side of FET for amplification and an input impedance matching circuit, a drain terminal is connected to a radio frequency signal output terminal by way of an output impedance matching circuit and a DC cut capacitor at output side of FET for amplification;

wherein a source terminal of a field effect transistor for bypass of amplifier is connected at the junction of the input side capacitor and the input impedance matching circuit by way of a DC cut

capacitor at source side of FET for bypass, a drain terminal of the field effect transistor for bypass of amplifier is connected at the junction of the drain terminal of the field effect transistor for signal amplification and the output impedance matching circuit by way of a DC cut capacitor at drain side of FET for bypass;

wherein the drain terminal of field effect transistor for input impedance correction is connected at the junction of the input impedance matching circuit and a DC cut capacitor at input side of FET for amplification by way of a first FET side DC cut capacitor for correction and a first FET side resistor for correction, a source terminal of the field effect transistor for input impedance correction is connected to the ground by way of a first FET side bypass capacitor for correction;

wherein a drain terminal of a field effect transistor for output impedance correction is connected at the junction of the drain terminal of the field effect transistor for signal amplification and the output impedance matching circuit by way of a second FET side DC cut capacitor for correction and a second FET side resistor for correction, a source terminal of the field effect transistor for output impedance correction is connected to the ground by way of a second FET side bypass capacitor for correction;

wherein each gate terminal of the field effect transistor for bypass of amplifier, the field effect transistor for input impedance correction, and the field effect transistor for output impedance correction is connected to the ground by way of each resistor;

wherein each drain terminal and source terminal of the field effect transistor for bypass of amplifier, the field effect transistor for input impedance correction, and the field effect transistor for output

impedance correction are connected to a first control voltage application terminal by way of each resistor;

wherein a source terminal of the field effect transistor for signal amplification is connected to a second gate terminal and a drain terminal of field effect transistor for bias SW by way of a inductor, this source terminal is connected to the ground by way of a capacitor; and

wherein a source terminal of the field effect transistor for bias SW is connected to the ground by way of a self-bias resistor, a gate terminal is connected to a second control voltage application terminal by way of a gate bias resistor.

3. Variable gain amplifier of Claim 2, wherein a plurality of any one of said field effect transistor for bypass of amplifier, said field effect transistor for input impedance correction, and the field effect transistor for output impedance correction are connected in series.

4. Variable gain amplifier for amplifying the radio frequency signal by using a field effect transistor for signal amplification,

wherein an amplifier bypass means comprising a field effect transistor for bypass of amplifier is connected parallel to the field effect transistor for signal amplification,

wherein a field effect transistor for bias SW for controlling the operation of this transistor is connected to the source terminal side of the field effect transistor for signal amplification, and

wherein a second gate terminal of the field effect transistor for signal amplification is connected at the junction of the source terminal of the field effect transistor for bias SW and self-bias resistor.

5. Variable gain amplifier for amplifying the radio frequency signal by using a field effect transistor for signal amplification,

wherein the field effect transistor for signal amplification is of dual gate type, a first gate terminal is connected to a radio frequency signal input terminal by way of a first DC cut capacitor and an input impedance matching circuit, and a drain terminal is connected to a radio frequency signal output terminal by way of an output impedance matching circuit and a second a DC cut capacitor;

wherein a source terminal of a field effect transistor for bypass of amplifier is connected at the junction of the first DC cut capacitor and the input impedance matching circuit by way of a third DC cut capacitor, and a drain terminal of the field effect transistor for bypass of amplifier is connected at the junction of the drain terminal of the field effect transistor for signal amplification and the output impedance matching circuit by way of a fourth DC cut capacitor;

wherein each gate terminal of the field effect transistor for signal amplification and field effect transistor for bypass of amplifier is connected to the ground by way of each resistor, a source terminal of the field effect transistor for signal amplification is connected to a drain terminal of a field effect transistor for bias SW by way of an inductor, said drain terminal is connected to the ground by way of a capacitor;

wherein a second gate terminal of the field effect transistor for signal amplification and the source terminal of the field effect transistor for bias SW are mutually connected, and a self-bias resistor and a bypass capacitor are connected between the junction and the ground;

wherein a gate terminal of the field effect transistor for bias

SW is connected to a second control voltage application terminal by way of a gate bias resistor; and

wherein the drain terminal and the source terminal of the field effect transistor for bypass of amplifier are connected to a first control voltage application terminal by way of each resistor.